09/966022

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No.:     6,954,773

Issue Date:     October 11, 2005

Inventor(s):    Jianwei LIU

Title:          PROVIDING AN ADDER WITH A CONVERSION CIRCUIT IN A SLACK
                PROPAGATION PATH (AS AMENDED)

Docket No.:     MP1444

                130200

## REQUEST FOR CERTIFICATE OF CORRECTION UNDER RULE 323

Certificate
MAR 1 4 2007
of Correction

Commissioner for Patents
Office of Patent Publications
ATTN:  Certificate of Correction Branch
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

It is respectfully requested that a Certificate of Correction be issued in order to correct the

error(s) specified in the attached copy of Certificate of Correction Form PTO-1050.

The corrections address mistakes that are clerical, typographical, and of minor character.

None of the corrections constitute new matter or require reexamination.

Proper antecedent basis was provided for "an adder circuit" recited in claims 1-6 and 12-16.

After correction, claim 1 recites "the adder circuit" in col. 8, line 29 referring back to "An adder

circuit" in col. 8, line 18. Claims 2-6 and 12-16 are similarly corrected. Because later references

back to "an adder circuit" were corrected to provide proper antecedent basis, no new matter is added

and reexamination is not required.

MAR 1 4 2007

Proper antecedent basis was provided for "two signals A and B" recited in claims 1 and 17. After correction, claim 1 recites "A and B signals" in col. 8, lines 36-37 referring back to "two signals A and B" in col. 8, line 34. Claim 17 is similarly corrected. Because later references back to "two signals A and B" were corrected to provide proper antecedent basis, no new matter is added and reexamination is not required.

Proper antecedent basis was provided for "two signals X and Y" recited in claims 1-3, 5, 17 and 18. After correction, claim 1 recites "the X and Y signals" in col. 8, line 38 referring back to "two signals X and Y" in col. 8, line 37. Claims 2, 3, 5, 17 and 18 are similarly corrected. Because later references back to "two signals X and Y" were corrected to provide proper antecedent basis, no new matter is added and reexamination is not required.

Proper antecedent basis was provided for "the first binary number" and "the second binary number" in claim 17. After correction, claim 17 recites "a first binary number" and "the second binary number" in col. 9, lines 55-56 as the initial recitation. Because this was the first occurrence of these two terms "a first binary number" and "a second binary number" is proper. For claim 26, "a first and a second binary number" is changed to "a first binary number and a second binary number" for proper English. Changing "the" to "a" in claim 17 and changing "a first and a second binary number" to "a first binary number and a second binary number" in claim 26 adds no new matter and does not require reexamination.

Proper antecedent basis was provided for "the input carry" recited in claim 18. After correction, claim 18 recites "an input carry" in col. 9, line 66 as the initial recitation. Because this was the first occurrence of this term, "an input carry" is proper. Changing "the" to "an" here adds no new matter and does not require reexamination.

Proper antecedent basis was provided for "microprocessor circuit" recited in claims 19-22. After correction, claim 19 recites "A microprocessor as in claim 17" in col. 10, line 1 referring back to "A microprocessor" recited in claim 17 in col. 9, line 51. Claims 20-22 are similarly corrected. Because later references back to "microprocessor" were corrected from "microprocessor circuit" to provide proper antecedent basis, no new matter is added and reexamination is not required.

Our Check No. 190358 in the amount of One Hundred Dollars ($100.00) is attached in accordance with the provisions of 37 C.F.R. §1.323 and §1.20(a). In the event of any underpayment or overpayment, please debit or credit Deposit Account No. 15-0461 as needed in order to ensure prompt issuance of a Certificate of Correction. Two duplicate copies of this Request are attached.

Respectfully submitted,

James A. Oliff
Registration No. 27,075

Lea A. Nicholson
Registration No. 48,346

JAO:LAN/eks

Date: March 9, 2007

**OLIFF & BERRIDGE, PLC**
**P.O. Box 19928**
**Alexandria, Virginia 22320**
**Telephone: (703) 836-6400**

DEPOSIT ACCOUNT USE
AUTHORIZATION
Please grant any extension
necessary for entry;
Charge any fee due to our
Deposit Account No. 15-0461

MAR 1 4 2007.

# UNITED STATES PATENT AND TRADEMARK OFFICE
# CERTIFICATE OF CORRECTION

PATENT NO    :   6,954,773

DATED       :   October 11, 2005

INVENTOR(S)   :   Jianwei Liu

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Claim 1, col. 8, line 29, "the adder" should read --the adder circuit--.
Claim 1, col. 8, lines 36-37, "A and B outputs" should read --A and B signals--.
Claim 1, col. 8, line 38, "X and Y" should read --the X and Y signals--.
Claim 2, col. 8, line 40, "adder" should read --adder circuit-- and "X and Y" should read --the X and Y signals--.
Claim 3, col. 8, line 50, "adder" should read --adder circuit-- and "X and Y" should read --the X and Y signals--.
Claim 4, col. 8, line 60, "adder" should read --adder circuit--.
Claim 5, col. 8, line 61, "adder" should read --adder circuit--.
Claim 5, col. 8, line 63, "the X and Y outputs" should read --the X and Y signals--.
Claim 6, col. 8, line 66, "adder" should read --adder circuit--.
Claim 12, col. 9, line 25, "adder" should read --adder circuit--.
Claim 13, col. 9, line 27, "adder" should read --adder circuit--.
Claim 14, col. 9, line 29, "adder" should read --adder circuit--.
Claim 15, col. 9, line 47, "adder" should read --adder circuit--.
Claim 16, col. 9, line 49, "adder" should read --adder circuit--.
Claim 17, col. 9, lines 55-56, "the first binary number" should read --a first binary number-- and "the second binary number" should read --a second binary number--.
Claim 17, col. 9, lines 59-60, "the A and B outputs" should read --the A and B signals--.
Claim 17, col. 9, line 62, "X and Y" should read --the X and Y signals--.
Claim 18, col. 9, line 65, "the X and Y outputs" should read --the X and Y signals--.
Claim 18, col. 9, line 66, "the input carry" should read --an input carry--.
Claim 19, col. 10, line 1, "microprocessor circuit" should read --microprocessor--.
Claim 20, col. 10, line 6, " microprocessor circuit" should read --microprocessor--.
Claim 21, col. 10, line 12, " microprocessor circuit" should read --microprocessor--.
Claim 22, col. 10, line 17, " microprocessor circuit" should read --microprocessor--.
Claim 26, col. 10, lines 43-44, "a first and a second binary number" should be --a first binary number and a second binary number--.

MAILING ADDRESS OF SENDER:    OLIFF & BERRIDGE, PLC
P.O. Box 19928
Alexandria, Virginia 22320
Telephone: (703) 836-6400

PATENT NO.   6,954,773

No. of additional copies

0

MAR 1 4 2006